**Amendments to the Claims:**

This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

1. (Currently Amended) A method for securing data of a data carrier comprising: ~~A method for storing and/or changing a state information item of a memory containing a plurality of memory cells, wherein the memory cells assume an irreversible memory state as a result of a programming step, wherein the state information is represented by a number and/or position of memory cells existing or programmed in an irreversible memory state, said method comprising the steps presented in the following;~~

determining a current state of a memory, wherein the memory comprises a plurality of memory cells and wherein the current state of the memory is selected from the group consisting of an active state and a quiet state and wherein in the active state the data of the data carrier is accessible and wherein in the quiet state the data of the data carrier is inaccessible;

if the memory is in the active state, then determining a current state of a memory cell, wherein the current state of the memory cell is selected from the group consisting of a programmed state and an unprogrammed state; and ~~determining the state information by checking the memory state of the memory and~~

if the current state of the memory cell is the unprogrammed state, then selecting ~~an unprogrammed memory~~the memory cell and programming the selected memory cell ~~during~~to change ~~and/or for changing~~ the current state ~~information~~ of the memory cell to the programmed state, wherein the memory cell assumes an irreversible memory state as a result of the programming and wherein the memory enters the quiet state.

2. (Currently Amended) ~~A~~ The method according to claim 1~~, wherein,~~ further comprising, ~~-~~prior to determination of the ~~state information~~ current state of the memory, ~~an encryption of data and/or a verification~~verifying ~~of an access~~ authorization to access ~~to~~ the memory ~~is carried out~~.

3. (Currently Amended) ~~A~~ The method according to claim 1, wherein~~,~~ determining a current state of a memory comprises;

associating the active state with an even count of memory cells in the programmed state;

determining a count of memory cells in the programmed state;

if the count of memory cells in the programmed state is even, then determining the current state of the memory to be the active state; and

if the count of memory cells in the programmed state is odd, then determining the current state of the memory to be the quiet state.~~for determining the state information of the memory, a serial output of the memory is fed to a counter or a toggle flip-flop, whereby the number of memory cells programmed or in an irreversible memory state and/or the position of an unprogrammed memory cell is determined.~~

4. (Currently Amended) The method according to claim 1, wherein determining a current state of a memory comprises;

associating the active state with an odd count of memory cells in the programmed state;

determining a count of memory cells in the programmed state;

if the count of memory cells in the programmed state is odd, then determining the current state of the memory to be the active state; and

if the count of memory cells in the programmed state is even, then determining the current state of the memory to be the quiet state.

~~A method according to claim 3, wherein timing pulses are applied to memory and by verifying the timing pulses at the serial output of the memory a position of an unprogrammed memory cell is determined.~~

5. (Currently Amended) An integrated circuit for securing data stored in a data carrier comprising: ~~for storing and/or changing state information of a memory containing~~

-a memory comprising a plurality of memory cells, wherein the memory comprises a plurality of memory cells~~wherein the memory cells assume an irreversible memory state as a result of a programming step,~~;

a first logic circuit configured for determining a current state of the memory, wherein the current state of the memory is selected from the group consisting of an active state and a quiet state and wherein in the active state the data of the carrier is accessible and wherein in the quiet state the data of the carrier is inaccessible;

~~said integrated circuit containing a programming unit for programming the memory cells and~~

a feed-~~feed-logic circuit~~logic circuit, wherein the ~~said~~ feed-logic circuit ~~being provided~~is configured for:

receiving state information indicative of a current state of a memory cell, wherein the current state of the memory cell is selected from the group consisting of a programmed state and an unprogrammed state; and

if the current state of the memory is the active state and if the current state of the memory cell is the unprogrammed state, then selecting the memory cell; and

issuing a programming command to the programming unit to program the selected memory cell to change the state of the memory cell to the programmed state, wherein the memory cell assumes an irreversible memory state as a result of the programming and wherein the memory enters the quiet state. ~~for picking up and emitting data for programming and determining the state information of memory.~~

6. (Currently Amended) ~~An~~ The integrated circuit according to claim 5 further comprising:

a counter; and

a sequencing circuit, wherein the sequencing circuit is configured for:

providing a clock signal to a clock input of the integrated circuit via the counter;

receiving a serial output from the integrated circuit indicative of the state of each of the plurality of memory cells; and

issuing a stop count signal to the counter when a first memory cell in the unprogrammed state is detected, and

wherein the counter is configured to count the clock signals to produce a count indicative of the location of the first memory cell in the unprogrammed state.

~~, wherein a serial output of the feed-logic circuit interacts with an evaluation unit for determining the state information and for selecting an unprogrammed memory cell.~~

7. (Canceled)

8. (Currently Amended) ~~An~~ The integrated circuit according to ~~claim 6~~claim 5 further comprising a verification circuit, wherein the verification circuit is configured for, prior to determination of the current state of the memory, verifying authorization to access the memory ~~wherein additionally a circuit is provided for the verification and/or encryption of data~~.

9. (Currently Amended) An integrated circuit according to ~~claims~~ claim 5~~, wherein additionally a memory is provided for additional storage of preset data~~, wherein the data stored in the data carrier is selected from the group consisting of preset data and data ~~and/or data that can be~~ entered via an input device.

10. (Currently Amended) A data carrier ~~containing~~ comprising an integrated circuit according to claim 5.

11. (Original) A data carrier according to claim 10, wherein the data carrier is designed for contactless communication with a communication station.

12. (Previously Presented) A data carrier according to claim 10, wherein the data carrier is in the form of a tag or label.

13. (New) The integrated circuit of claim 5, wherein the active state is associated with an even count of memory cells in the programmed state and wherein the first logic circuit is configured for:

determining a count of memory cells in the programmed state;

if the count of memory cells in the programmed state is even, then determining the current state of the memory to be the active state; and

if the count of memory cells in the programmed state is odd, then determining the current state of the memory to be the quiet state.

14. (New) The integrated circuit of claim 5, wherein the active state is associated with an odd count of memory cells in the programmed state and wherein the first logic circuit is configured for:

determining a count of memory cells in the programmed state;

if the count of memory cells in the programmed state is odd, then determining the current state of the memory to be the active state; and

if the count of memory cells in the programmed state is even, then determining the current state of the memory to be the quiet state.